

AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

- 1 1. (original) An image sensor apparatus, comprising:
2 a pixel circuit for sensing image information;
3 a readout circuit coupled to said pixel circuit for reading out the
4 image information, said readout circuit including a capacitor and a switching
5 arrangement coupled to said capacitor for switching said capacitor into and out
6 of connection between each of first and second pairs of nodes of said readout
7 circuit.

- 1 2. (original) The apparatus of Claim 1, wherein said capacitor, when
2 connected between said first pair of nodes, stores charge for reducing noise
3 when reading out the image information.

- 1 3. (original) The apparatus of Claim 2, wherein said noise includes fixed-
2 pattern noise (FPN).

- 1 4. (original) The apparatus of Claim 2, wherein one of said first pair of
2 nodes is a low impedance node.

- 1 5. (original) The apparatus of Claim 4, wherein said low impedance node
2 is an output of said readout circuit for reading out the image information.

- 1 6. (original) The apparatus of Claim 1, wherein said capacitor, when
2 connected between said first pair of nodes, is for reading out the image
3 information.

1 7. (original) The apparatus of Claim 6, wherein said capacitor, when
2 connected between said second pair of nodes, stores charge for reducing noise
3 when reading out the image information.

1 8. (original) The apparatus of Claim 7, wherein one of said second pair
2 of nodes is a low impedance node.

1 9. (original) The apparatus of Claim 8, wherein said low impedance node
2 is an output of said readout circuit for reading out the image information.

1 10. (original) The apparatus of Claim 1, provided as a CMOS image
2 sensor, and wherein said capacitor is a poly/n-well capacitor.

1 11. (original) The apparatus of Claim 1, wherein said capacitor includes a
2 first capacitor plate for connection to a first node of each of said pairs and a
3 second capacitor plate for connection to a second node of each of said pairs,
4 and wherein said first node of said first pair is electrically distinct from said first
5 node of said second pair.

1 12. (original) The apparatus of Claim 11, wherein said second node of
2 said first pair is electrically distinct from said second node of said second pair.

1 13. (original) The apparatus of Claim 12, wherein each of said nodes of
2 said first and second pairs is electrically distinct from the remaining nodes of said
3 first and second pairs.

1 14. (original) The apparatus of Claim 1, wherein one of said nodes is a
2 low impedance node that serves as an output of said readout circuit.

1 15. (original) The apparatus of Claim 1, wherein said readout circuit
2 includes a buffer having an input coupled to said switching arrangement for
3 connection to said pixel circuit, said buffer having an output for outputting the
4 image information from said readout circuit.

1 16. (original) The apparatus of Claim 15, wherein said buffer output is one
2 of said nodes of said first pair and said buffer input is one of said nodes of said
3 second pair.

1 17. (original) The apparatus of Claim 1, wherein one of said nodes is a
2 reference voltage node and another of said nodes is a low impedance node.

1 18. (original) A method of controlling an image sensor apparatus
2 including a pixel circuit for sensing image information and a readout circuit
3 coupled to the pixel circuit for reading out the image information, comprising:
4 switching a capacitor into and out of connection between a first pair
5 of nodes of the readout circuit; and
6 switching the capacitor into and out of connection between a
7 second pair of nodes of the readout circuit.

1 19. (original) The method of Claim 18, including, when the capacitor is
2 connected between the first pair of nodes, storing charge in the capacitor for
3 reducing noise when reading out the image information.

1 20. (original) The method of Claim 19, including, when the capacitor is
2 connected between the second pair of nodes, reading out the image information.

1 21. (original) The method of Claim 18, including, when the capacitor is
2 connected between the first pair of nodes, reading out the image information.

1 22. (original) The method of Claim 18, wherein one of said switching
2 steps includes switching said capacitor into connection between a low
3 impedance node and a further node.

1 23. (original) The method of Claim 22, including using said low
2 impedance node as an output node for reading out the image information from
3 the readout circuit.

Claims added by this Amendment:

1 24. (new) A method of controlling an image sensor apparatus including
2 (1) a plurality of pixel circuits, each having a photodiode and supplied with power
3 having a first supply voltage, for sensing image information and providing as an
4 output in a readout period a sense voltage representative of the sensed image
5 information, and (2) a readout circuit supplied with power having a second supply
6 voltage, and including a buffer having an input and an output, coupled to receive
7 at an input in sequential readout periods the outputs of the pixel circuits and
8 provide as an output a sequence of pixel voltages corresponding to the
9 sequence of outputs of the pixel circuits, comprising, in each readout period, the
10 steps of:

11 switching a capacitor into a first configuration having connection
12 between the second supply voltage and the output of the buffer; and then

13 switching the capacitor into a second configuration having
14 connection between the output of a pixel circuit and the input of the buffer, such
15 that the capacitor, when the capacitor is in the first configuration a compensating
16 voltage is stored therein including voltage components incidental to the readout
17 of the pixel voltage, and when the capacitor is in the second configuration the
18 incidental voltage components are canceled.

1 25. (new) A method according to Claim 24, wherein the pixel circuit
2 comprises a MOS transistor having a source, a gate and a drain, the source
3 being connected by way of a first switch to the input of the readout circuit, the
4 drain being connected to the first supply voltage and the gate being connected to
5 the common connection node of first terminals of a second switch and the
6 photodiode, the other terminal of the second switch being connected to the first
7 reference voltage and the other terminal of the photodiode being connected to
8 ground.